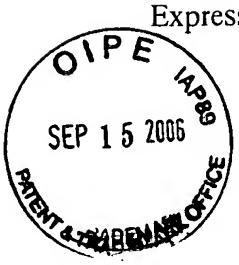
09-18-06 IFW

Express Mail No. EV 829 952 999 US



PATENT
Atty. Docket No. PWRSP009/PWR-026995

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Frank Anthony Doljack et al.	Art Unit:	2831
Serial No.:	10/781,571	Examiner:	Ha, Nguyen T.
Filed:	February 17, 2004		
For:	ACTIVE BALANCING MODULAR CIRCUITS		

LETTER

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Enclosed is a copy of the Declaration of Prior Invention (37 C.F.R. § 1.131) of inventor Frank Anthony Doljack which was originally filed June 19, 2006 with the Amendment filed on the same date for the above referenced matter. The attached Declaration includes Appendices A-E that were inadvertently not attached to the Declaration as originally submitted. The declaration is otherwise unchanged.

Applicants respectfully request that the Declaration be considered with the Amendment filed June 19, 2006.

Respectfully Submitted,

Bruce T. Atkins
Registration No. 43,476
ARMSTRONG TEASDALE LLP
One Metropolitan Square, Suite 2600
St. Louis, Missouri 63102-2740
(314) 621-5070

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Frank Anthony Doljack et al.	Art Unit:	2831
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CERTIFICATE OF MAILING BY EXPRESS MAIL TO THE COMMISSIONER OF PATENTS AND TRADEMARKS

Express Mail mailing label number: **EV 829 952 999 US**

Date of Mailing: September 15, 2006

I certify that the documents listed below:

- Certificate of Express Mailing (1 page)
- Letter (1 page)
- Declaration of Prior Invention of Frank Anthony Doljack (4 pages)
- Appendices A-E (31 pages)
- Return Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above in an envelope addressed to: Mail Stop: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Bruce T. Atkins, Reg. No. 43,476
ARMSTRONG TEASDALE LLP
One Metropolitan Square, Suite 2600
St. Louis, MO 63102-2740
(314) 621-5070

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Doljack et al.	Art Unit:	2831
Serial No.:	10/781,571	Examiner:	Ha, Nguyn T.
Filed:	February 17, 2004		
For:	ACTIVE BALANCING MODULAR CIRCUITS		

DECLARATION OF PRIOR INVENTION

(37 C.F.R. § 1.131)

Hon. Assistant Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Frank Anthony Doljack, whose address is 750 Montevino Dr., Pleasanton, California declares as follows:

1. This declaration is to establish actual reduction to practice of the invention claimed in the above-referenced application at a date prior to April 25, 2003.

2. I have reviewed and understand the patent application referenced in the caption above (hereinafter the "Subject Application"), including the specification, abstract, drawings and claims therefor.

3. I am an inventor of the invention described and claimed in the Subject Application.

4. I have reviewed United States Patent No. 6,806,686 filed on April 25, 2003 (hereinafter the "Antedated Reference"), which has been relied upon to reject at least one claim of the Subject Application.

5. The invention claimed in the Subject Application was reduced to practice before April 25, 2003 which is the filing date of the Antedated Reference.

6. As evidence that the invention was reduced to practice before the filing date of the Antedated Reference, attached hereto as Appendix A is a true and accurate copy of a computer screen shot taken from a computer having a directory of files related to development of the invention.

7. As shown in Appendix A, the directory includes a number of files in a subdirectory labeled "Balancing" that pertain to the development of the invention, and one of the files in the Balancing subdirectory is named "Unitcell1.bmp".

8. I created the file named "Unitcell1.bmp".

9. Attached hereto as Appendix B is a true and accurate printout of the Unitcell1.bmp file. As seen from Appendix B, the file includes a circuit schematic of capacitors connected in series, with active balancing elements connected to the capacitors.

10. More specifically, the drawing of the Unitcell1.bmp illustrates a circuit module having inductor-free circuitry for controlling voltage imbalances between a pair of capacitors connected in a series arrangement. The module includes a first terminal configured for connection to a positive plate of the first capacitor; a second terminal configured for connection to a negative plate of the first capacitor and to a positive plate of the second capacitor; and a third terminal configured for connection to a negative plate of the second capacitor. An active element is integrated within the inductor-free circuitry between the first, second, and third

terminals and is adapted to substantially balance the voltage imbalances between the pair of capacitors. The active element has power connections to the first and third terminals.

11. Attached hereto as Appendix C is a true and accurate screen shot taken the computer showing the Properties of the Unitcell1.bmp file. As seen in Appendix C, the Unitcell1.bmp file was created on January 13, 2003.

12. As further evidence that the claimed invention was reduced to practice before the filing date of the Antedated Reference, attached hereto as Appendix D are true and accurate copies of documents, including circuit schematics and notes relating to construction and testing of models or prototypes of the invention that were actually constructed.

13. As seen in Appendix D, a working model or prototype of the invention was constructed on February 27, 2003 and was tested on the same day. Further embodiments of the invention were also constructed and tested at various times and dates between March 3, 2003 and March 20, 2003 as Appendix D demonstrates.

14. In Appendix D, handwritten notes are my own and the notes were made as of the date indicated in the documents.

15. As is evident from Appendix D, the constructed embodiments of the invention actually worked for their intended purpose to balance voltages across capacitors connected in series.

16. As still further evidence of a reduction to practice of the invention, attached hereto as Appendix E are drawings (both computer generated and hand sketches) of printed circuit board artwork, and information pertaining to components for the active balancing element used to construct models and/or prototypes of the invention at a date prior to April 25, 2003.

17. The computer generated drawings include footers indicating the dates that the drawings were printed. As seen from Appendix E, all of the computer drawings were printed at a date prior to April 25, 2003.

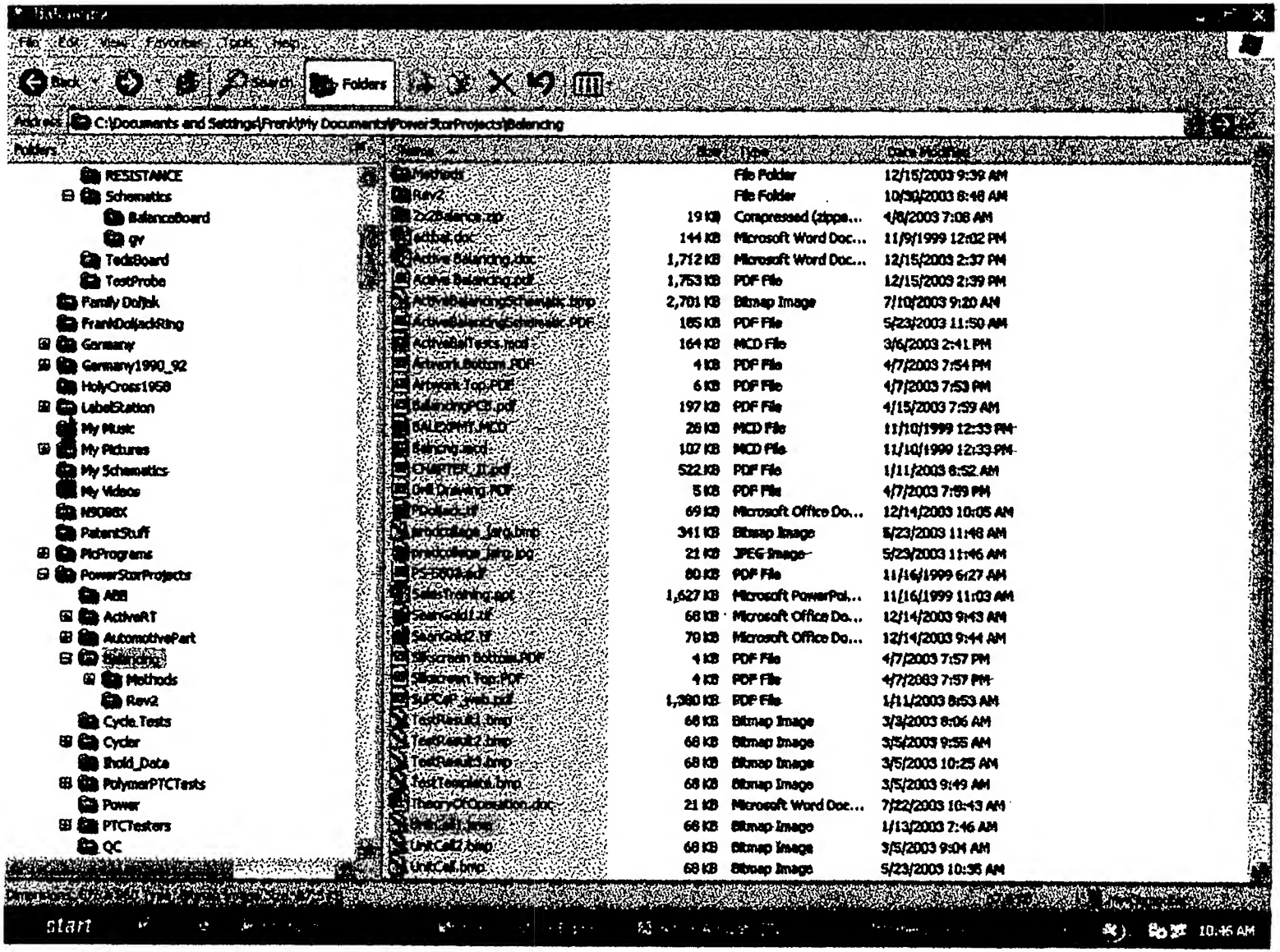
18. All activities documented in the factual evidence of Appendices A through E occurred in the United States.

19. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on Information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

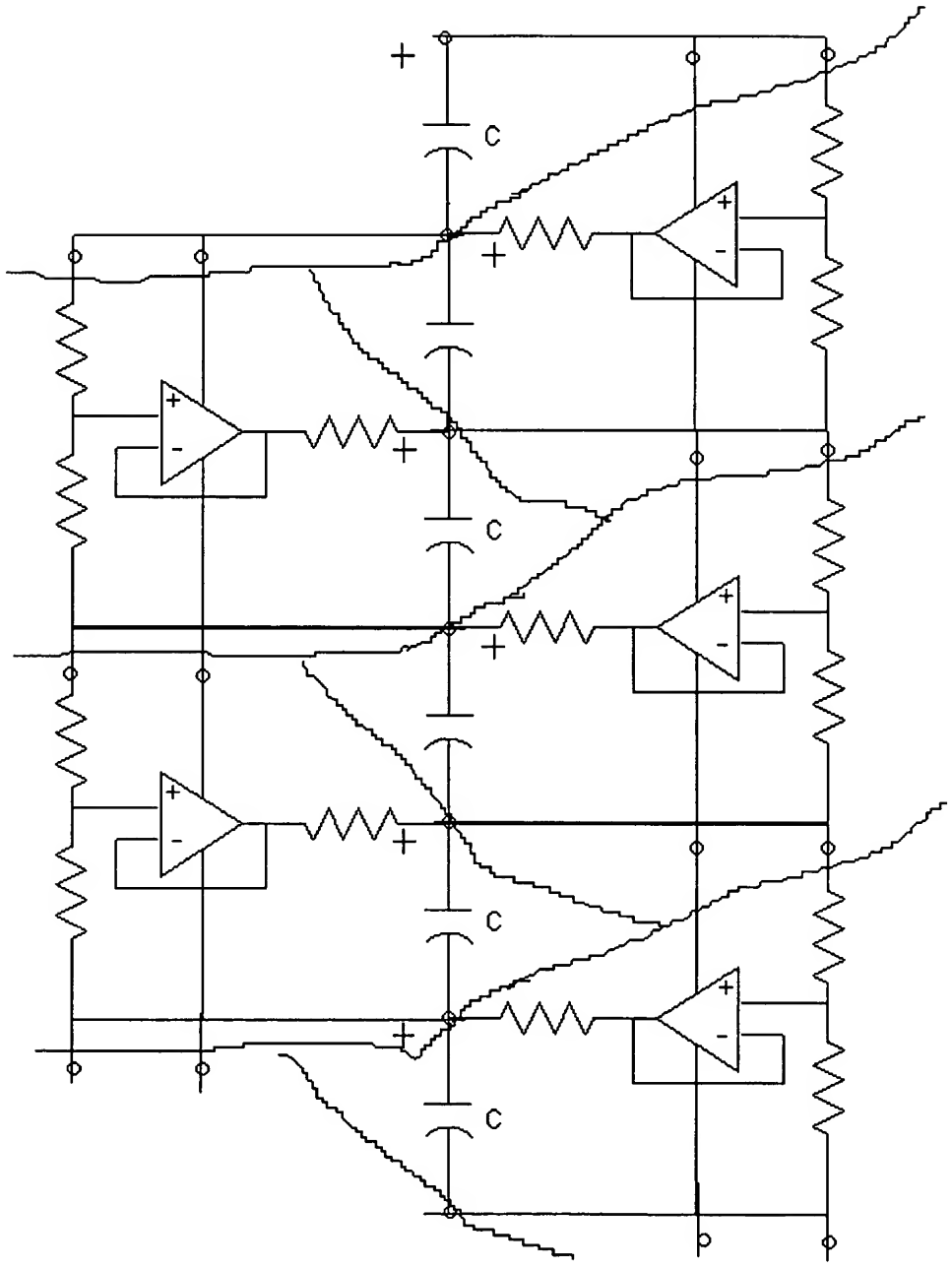
Frank Anthony Doljack Jun 16, 2006

Frank Anthony Doljack **(Date)**

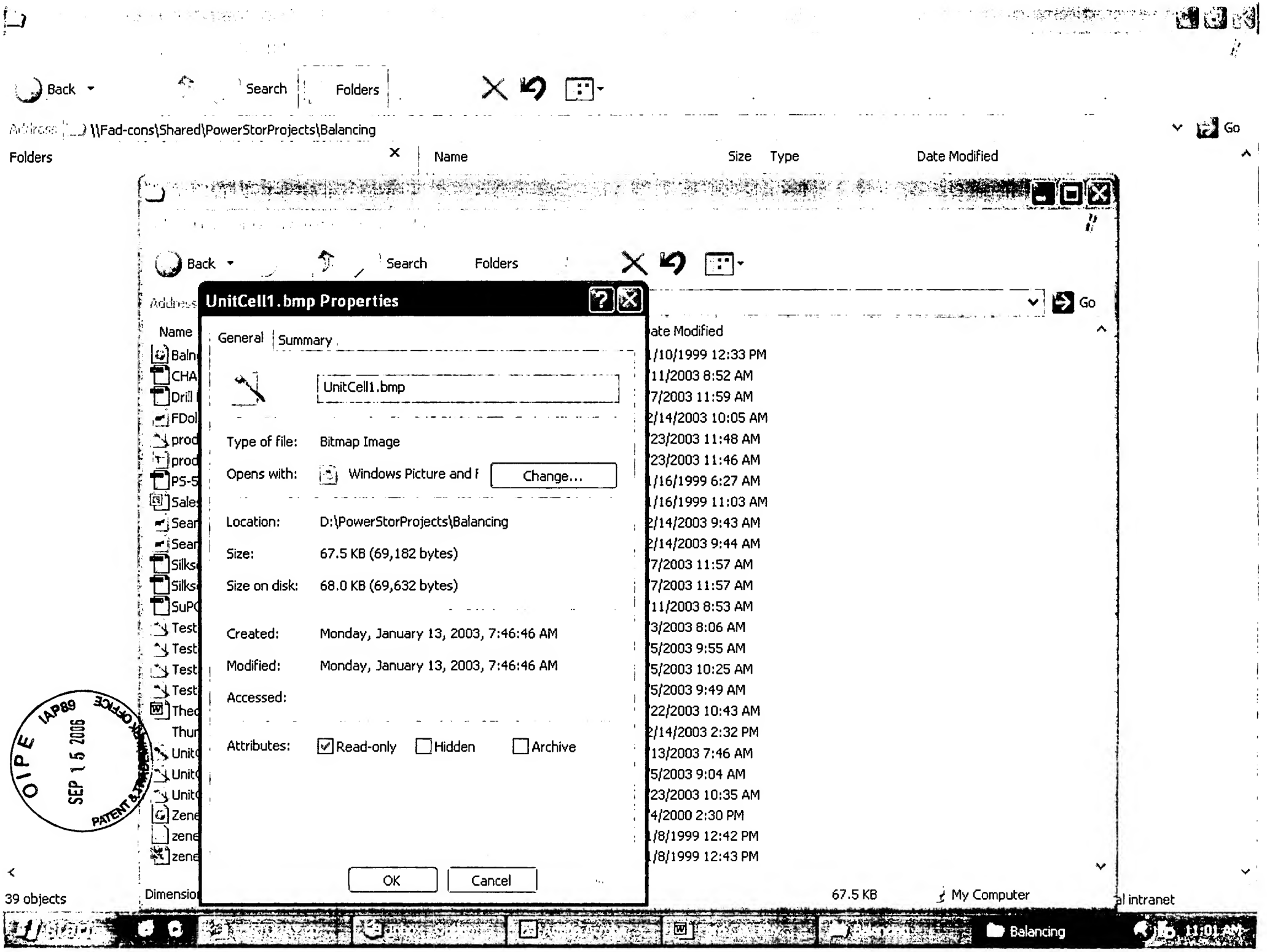
APPENDIX A



APPENDIX B


C
C
C
C

APPENDIX C



APPENDIX D

2/27/03

~~1 minute~~ after charging to 12.5V at 4.10p.m.

~~1) 2.495~~

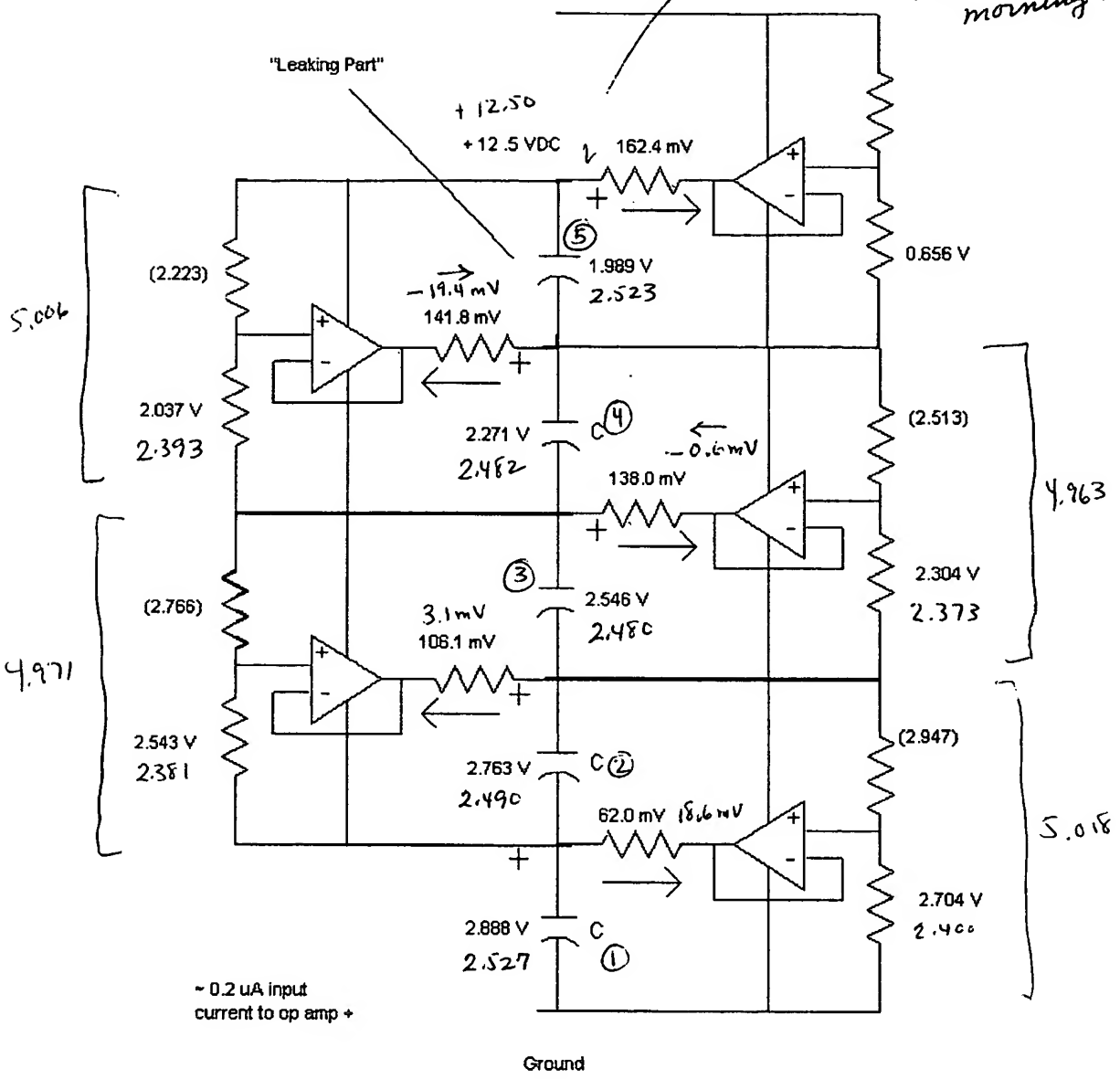
1 minute	5 minute	30 minute	1hr	2hr
1) 2.495	1) 2.455	1) 2.444	1) 2.461	1) 2.511
2) 2.465	2) 2.470	2) 2.473	2) 2.484	2) 2.523
3) 2.431	3) 2.454	3) 2.488	3) 2.504	3) 2.544
4) 2.569	4) 2.538	4) 2.527	4) 2.537	4) 2.530
5) 2.538	5) 2.580	5) 2.557	5) 2.496	5) 2.356

2/28/03

9.05am	11.05am	1.05pm
1) 2.862	1) 2.875	1) 2.883
2) 2.763	2) 2.765	2) 2.765
3) 2.555	3) 2.550	3) 2.546
4) 2.282	4) 2.276	4) 2.273
5) 1.993	5) 1.989	5) 1.988

Stack was also discharged on Friday and experiment restarted.

This point was disconnected on Friday and voltages re-measured Monday morning. 3/3/03



Over the weekend the circuit appears to be working to balance all voltages.

Frank,

Active Balancing Test charge at 12.5V

Recho Result Recharge at 3/3/03

3/3/03

2 min after recharge at 11am

1) 2.575
2) 2.461
3) 2.399
4) 2.599
5) 2.499

12 p.m

1) 2.521
2) 2.463
3) 2.441
4) 2.527
5) 2.551

3 p.m

1) 2.519
2) 2.478
3) 2.468
4) 2.490
5) 2.548

5 p.m

1) 2.521
2) 2.484
3) 2.475
4) 2.486
5) 2.537

3/4/03

9.15am

1) 2.526
2) 2.490
3) 2.480
4) 2.483
5) 2.524

2.45 p.m

1) 2.527
2) 2.490
3) 2.479
4) 2.483
5) 2.524

5.20 p.m

1) 2.527
2) 2.490
3) 2.480
4) 2.483
5) 2.523

3/5/03

8:45 am

1) 2.535
2) 2.498
3) 2.489
4) 2.490
5) 2.539

Emily
3/4/03

SR 4:36 PM 3/5/03

4:41 PM

1) 2.554
2) 2.467
3) 2.386
4) 2.596
5) 2.494

9:00 AM 3/10/03

1) 2.543
2) 2.524
3) 2523
4) 2.472
5) 2.427

8:35 AM 3/6/03

1) 2.547
2) 2.478
3) 2.418
4) 2.548
5) 2.513

5:00 PM

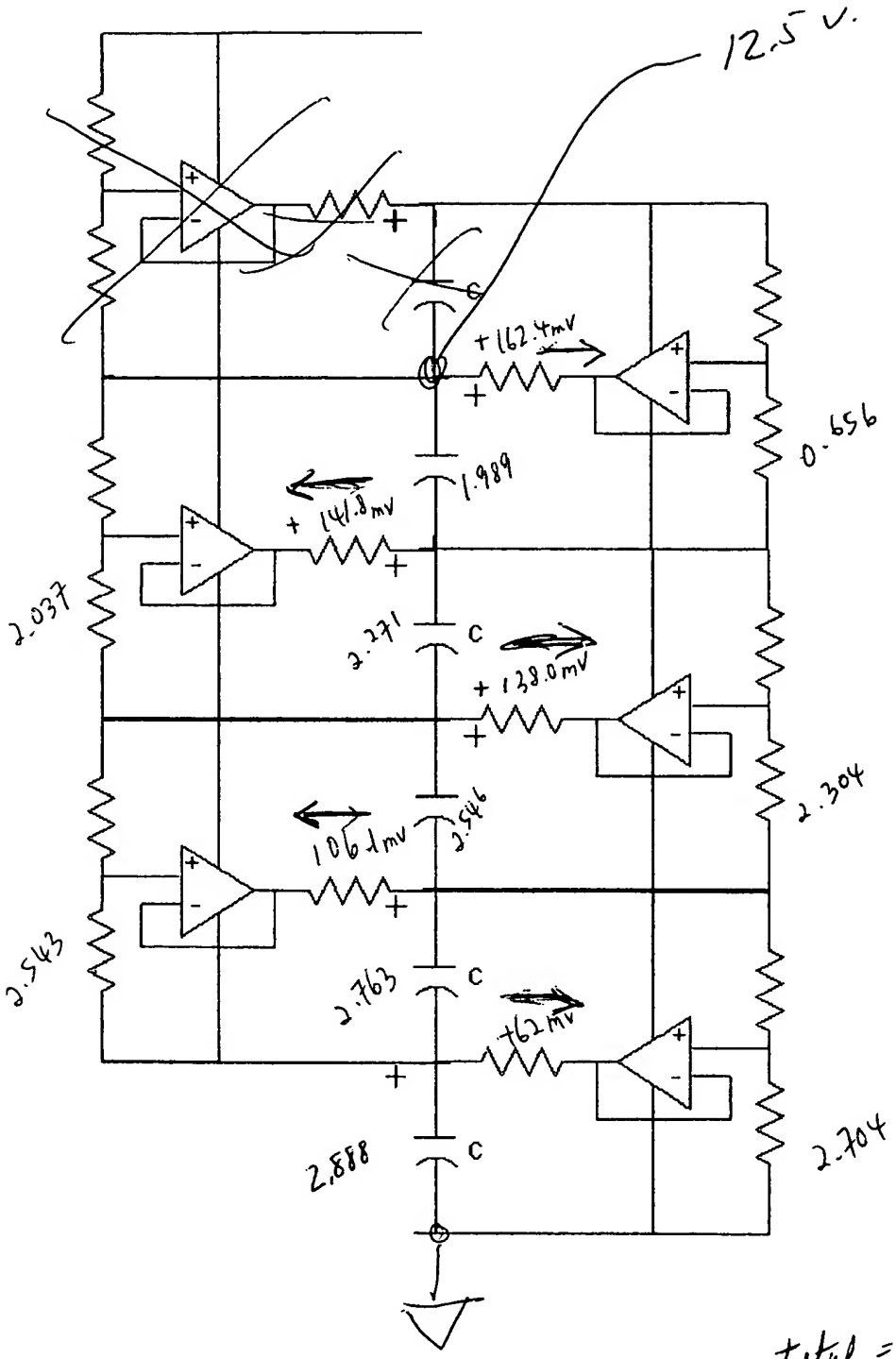
1) 2.758
2) 2.752
3)
4)
5) 2.

9:15 am 3/7/03

1) 2.550
2) 2.548
3) 2.555
4) 2.479
5) 2.354

2:50 PM

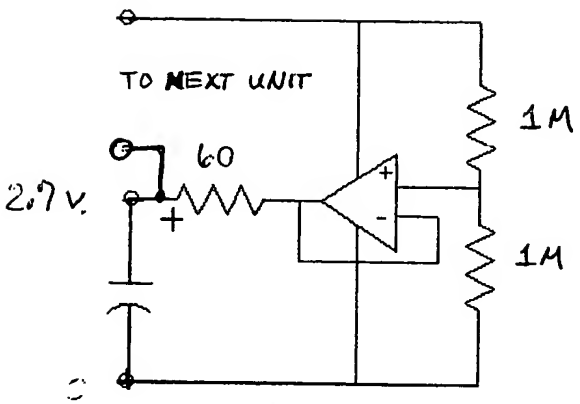
1) 2548
2) 2.549
3) 2.551
4) 2.477
5) 2.365



total = 12.459 V.

2000 F part has 1 μA/F leakage
after 300 hours

3PA334



1 1/2" for 200 F part

smaller part is 7/8" spacing

$$\frac{(2.75)^2}{60} = 1/8 \text{ watt} \quad (\text{use } 1/4 \text{ watt})$$

2.7
2.7
13.5

~ 4:36 PM 3/5/03

4:41 PM

1) 2.554
2) 2.467
3) 2.386
4) 2.596
5) 2.494

9:00 AM 3/10/03

1) 2.543
2) 2.524
3) 2.523
4) 2.472
5) 2.427

8:35 AM 3/6/03

1) 2.547
2) 2.478
3) 2.418
4) 2.548
5) 2.513

4.45 p.m 3/10/03

1) 2.542
2) 2.522
3) 2.521
4) 2.471
5) ~~2.423~~ 2.432

5:00 PM

1) 2.758
2) 2.752
3)
4)
5) 2.

9:15 am 3/7/03

1) 2.550
2) 2.548
3) 2.555
4) 2.479
5) 2.354

4:30 pm 3/11/03

1) 2.540
2) 2.518
3) 2.514
4) 2.469
5) 2.445

2:50 PM

1) 2.548
2) 2.549
3) 2.551
4) 2.477
5) 2.365

9:15 am 3/12/03

1) 2.541
2) 2.517
3) 2.511
4) 2.468
5) 2.453

5.00 3/12/03

1) 2.540
2) 2.516
3) 2.509
4) 2.467
5) 2.456

3/13/03 9.15am

1) 2.540
2) 2.515
3) 2.506
4) 2.466
5) 2.462

3/13/03 5 p.m

1) 2.540
2) 2.513
3) 2.505
4) 2.465
5) 2.465

3/14/03 9am

1) 2.540
2) 2.513
3) 2.502
4) 2.465
5) 2.469

3/14/03 5 p.m

1) 2.540
2) 2.512
3) 2.501
4) 2.464
5) 2.471

3/17/03 9.40am

1) 2.541
2) 2.571
3) 2.494
4) 2.462
5) 2.482

3/17/ 5 p.m

1) 2.540
2) 2.510
3) 2.493
4) 2.461
5) 2.487

3/18/ 9:15am

1) 2 540
2) 2.510
3) 2.491
4) 2 461
5) 2.485

3/18/ 5 p.m

1) 2.542
2) 2.512
3) 2.492
4) 2.463
5) 2.489

3/19 9.15am

1) 2 542
2) 2.512
3) 2.491
4) 2.463
5) 2.491

3/19 5 p.m

1) 2.543
2) 2.512
3) 2.491
4) 2.463
5) 2.492

3/20/ 9.30am

1) 2.542
2) 2.512
3) 2.490
4) 2.463
5) 2.485

2/27/03 started 4:10 PM, 2/28/03 ended after 1:05 PM

Devices 1 thru 5, Voltage in VDC

V :=

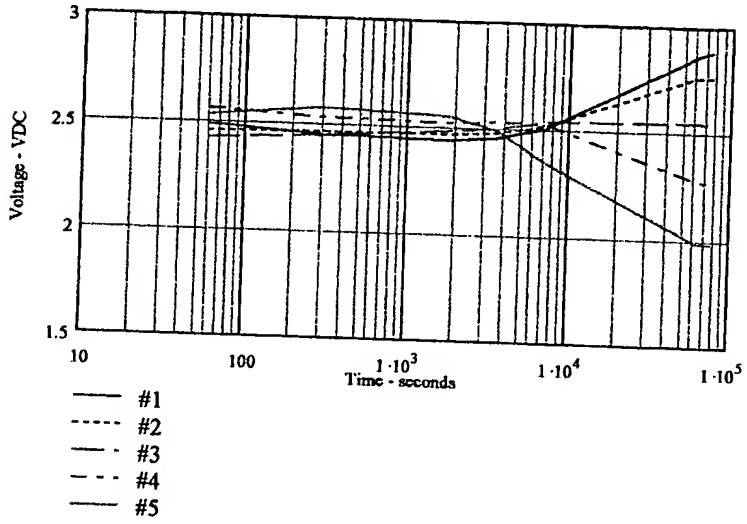
	0	1	2	3	4
0	2.495	2.455	2.444	2.461	2.511
1	2.465	2.47	2.473	2.484	2.523
2	2.431	2.454	2.488	2.504	2.544
3	2.569	2.538	2.527	2.537	2.53
4	2.538	2.58	2.557	2.496	2.35

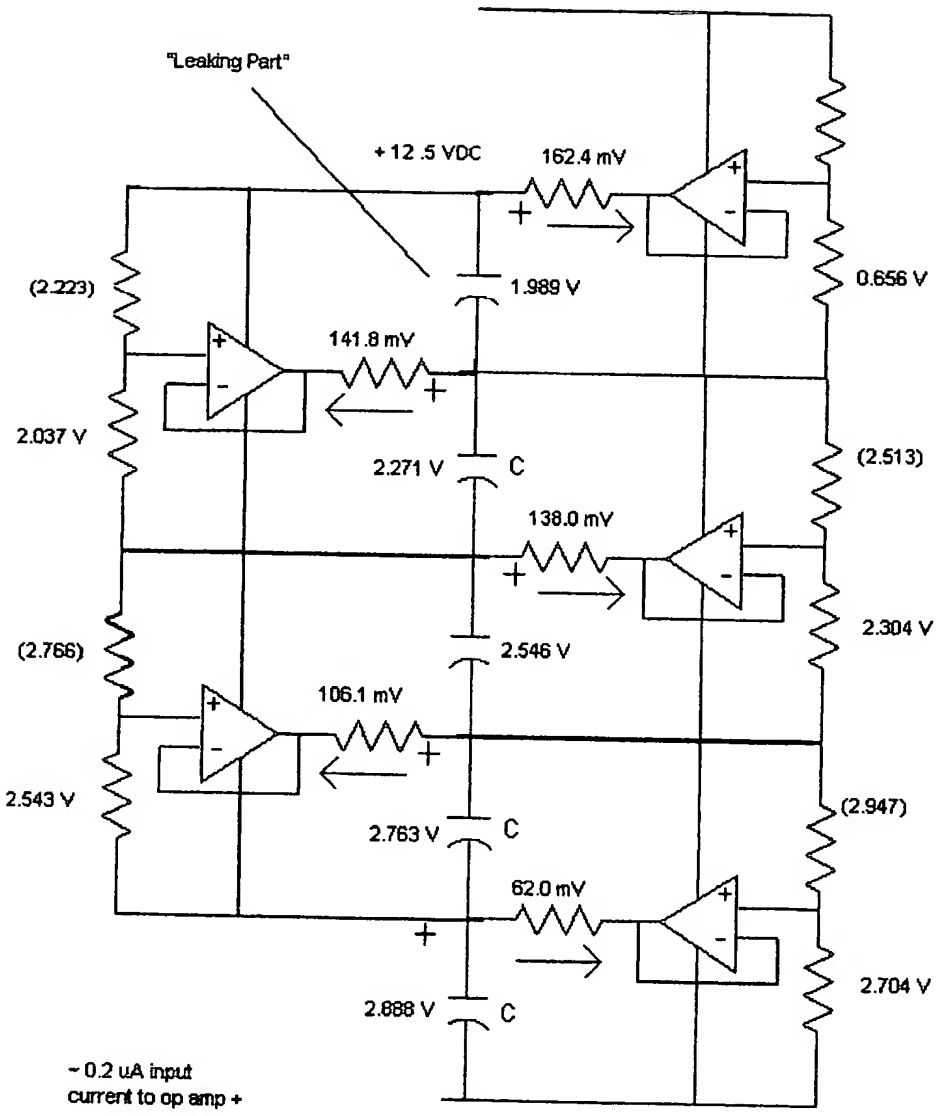
Elapsed time of measurement in seconds

T :=

	0	1	2	3	4
0	60	300	1800	3600	7200

$i := 0, 1 .. 7$

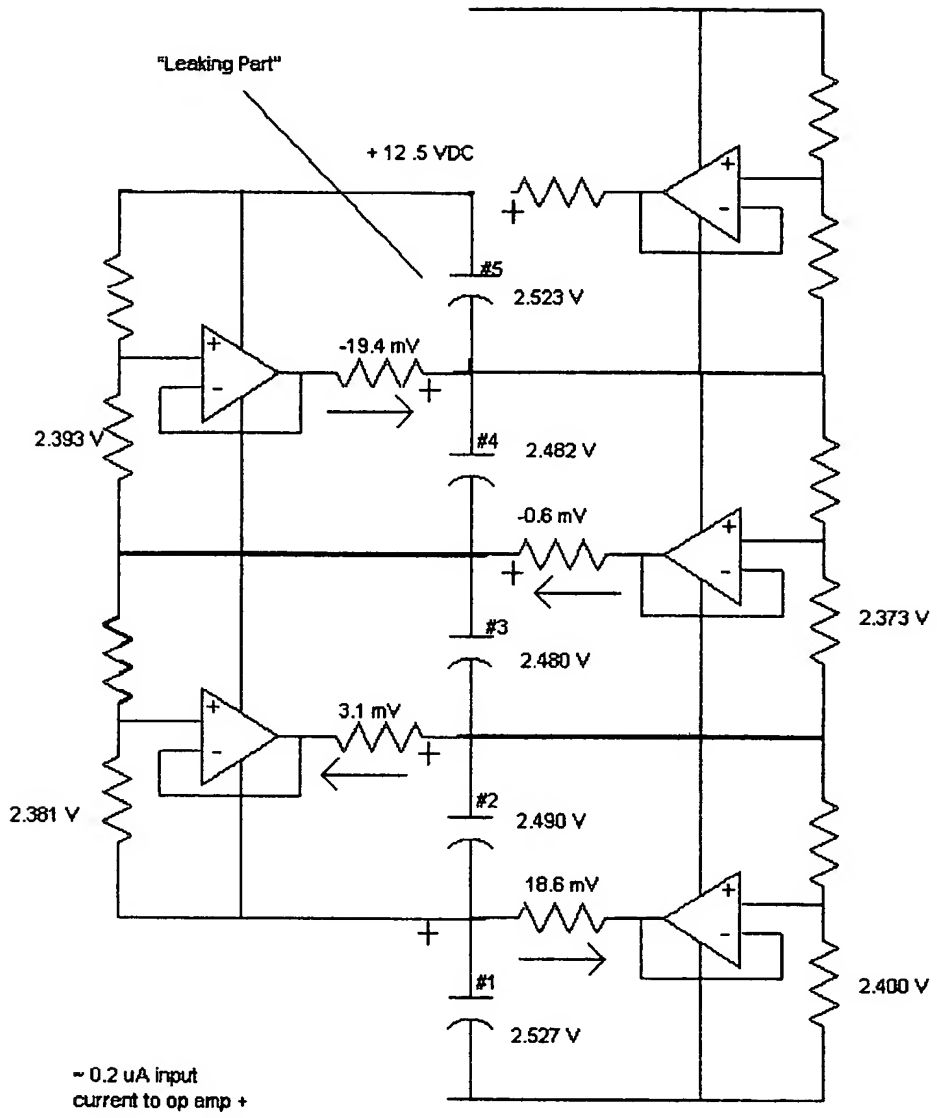




(Arrows show direction of current flow.)

Analysis: Device 5 is at the top of the above schematic. This schematic depicts the state of the circuit at the end of the test. Note that the theory of operation uses four op amps to balance five capacitors. The last op amp in the upper right is not intended to operate. However, it is connected to the device 5 and appears to be attempting to drive device 5 to low voltage. It was disconnected and the test restarted after discharge and recharged over the weekend. The Monday morning results are shown below.

Monday morning, 3/3/03, test results:



Analysis: The voltage states shown above indicate that the capacitor voltages are being balanced by the op amps. Note that the non-operational op amp is disconnected and cannot influence circuit operation.

Test restarted at 11 AM on 3/3/03:

Devices 1 thru 5, Voltage in VDC

V :=

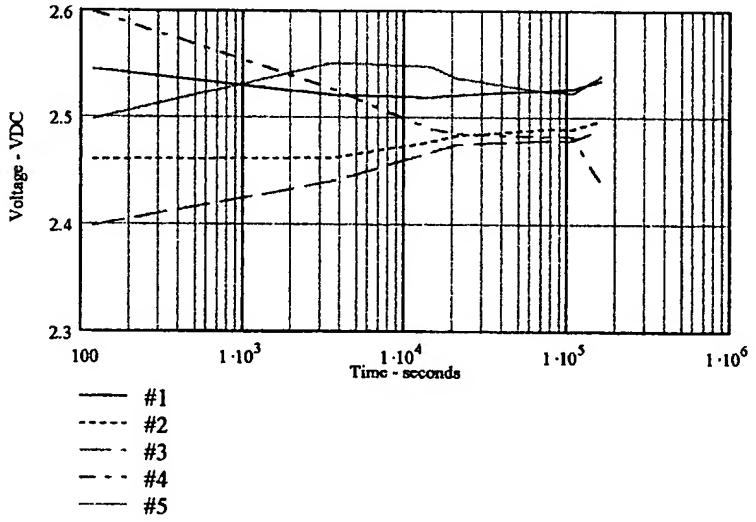
	4	5	6	7	8
0	2.526	2.527	2.527	2.535	
1	2.49	2.49	2.49	2.498	
2	2.48	2.479	2.48	2.489	
3	2.483	2.483	2.483	2.44	
4	2.524	2.524	2.523	2.539	

Elapsed time of measurement in seconds

T :=

	3	4	5	6	7
0	21600	79210	97250	$1.08 \cdot 10^5$	$1.62 \cdot 10^5$

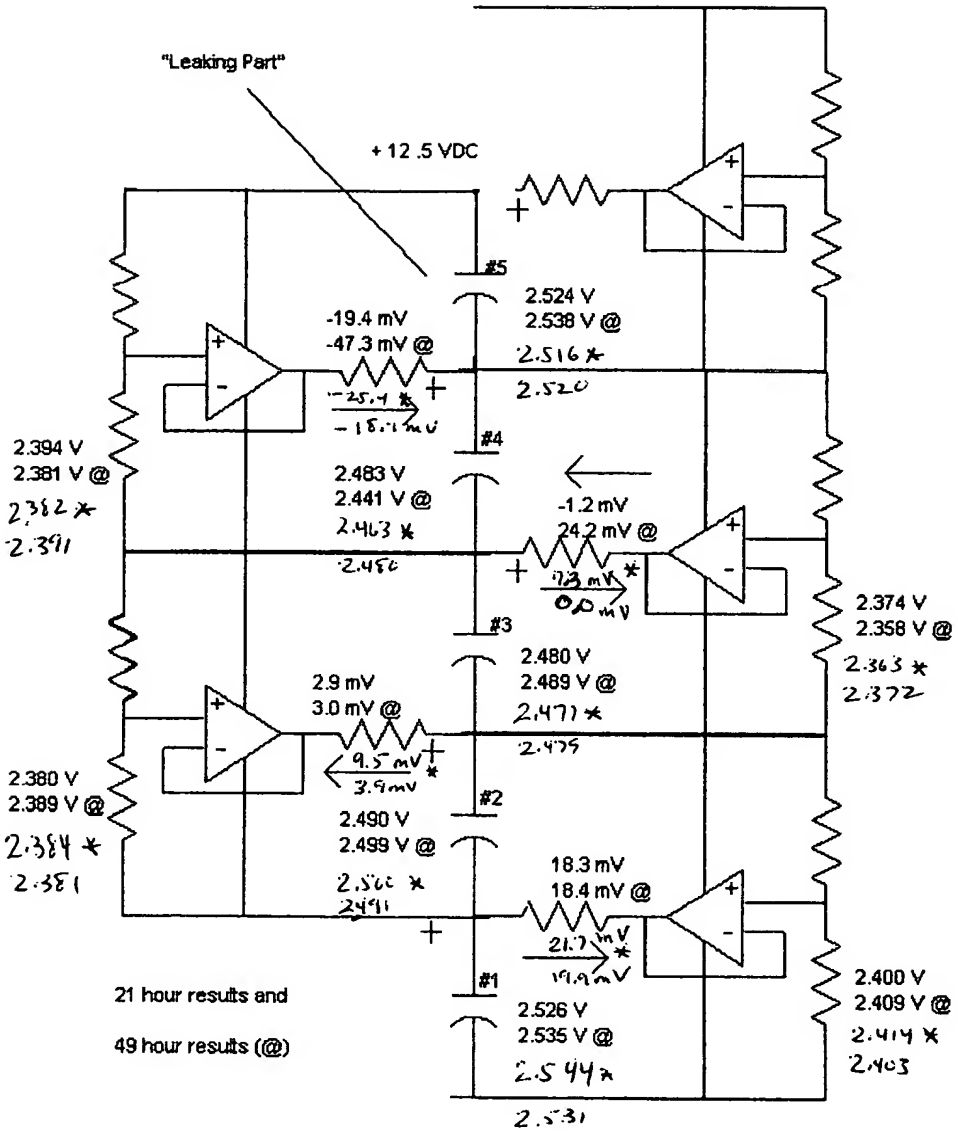
$i := 0, 1 .. 7$



on 4:36 PM 3/5/03

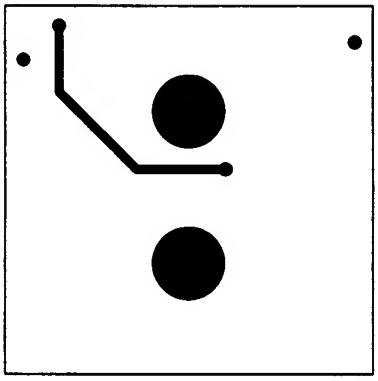
4:41 PM

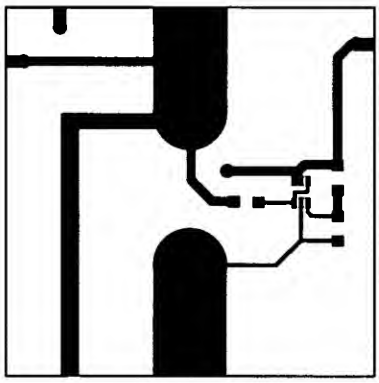
1 2.554
2 2.467
3 2.386
4 2.596
5 2.494

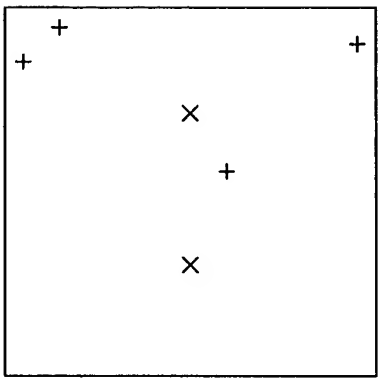

"Leaking Part"
+ 12 .5 VDC
#5
2.524 V
2.538 V @
2.516 *
2.520
-19.4 mV
-47.3 mV @
#4
2.483 V
2.441 V @
2.463 *
2.480
2.394 V
2.381 V @
2.382 *
2.391
-1.2 mV
24.2 mV @
#3
2.480 V
2.489 V @
2.471 *
2.479
2.374 V
2.358 V @
2.363 *
2.372
2.9 mV
3.0 mV @
#2
2.490 V
2.499 V @
2.491
2.380 V
2.389 V @
2.384 *
2.381
18.3 mV
18.4 mV @
#1
2.526 V
2.535 V @
2.544
2.531
2.400 V
2.409 V @
2.414 *
2.403
21 hour results and
49 hour results (@)

* 10:45 AM 3/5/03

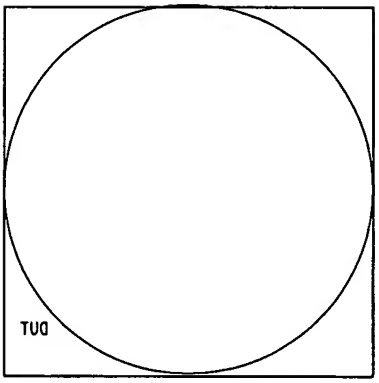
APPENDIX E

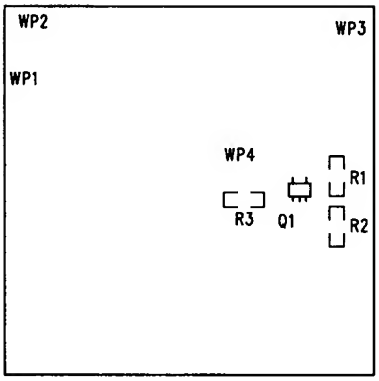




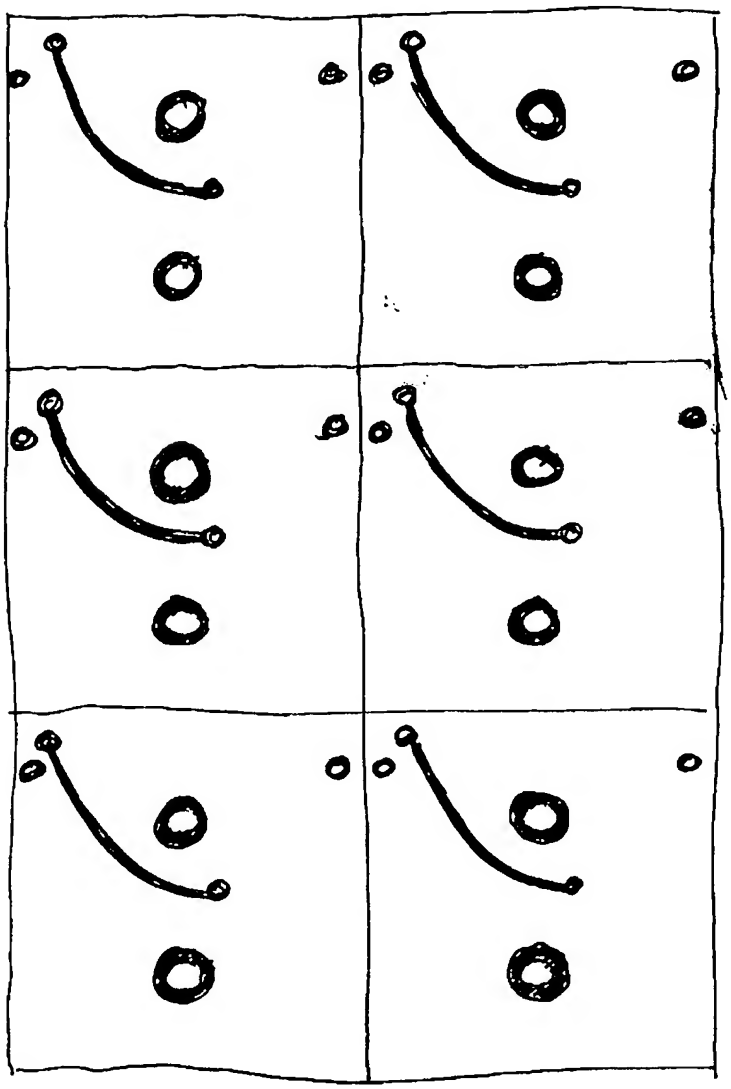


SIZE	QTY	SYM	PLTD
0.045	4	+	PLTD
0.201	2	×	PLTD


TUO

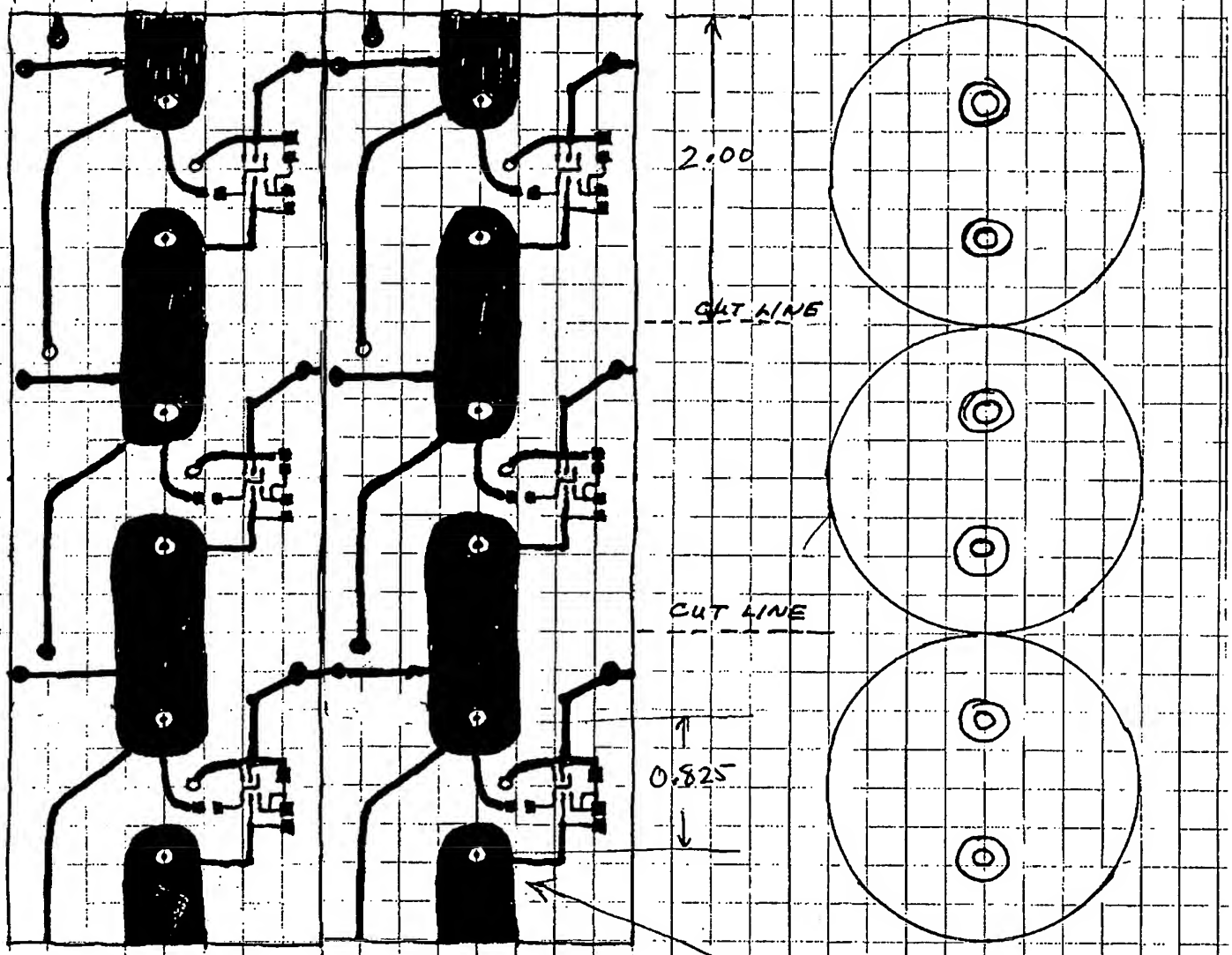

WP2
WP3
WP1
WP4
R1
R3
Q1
R2

BOTTOM ARTWORK



dimensions in inches.

TOP ARTWORK



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	+7V
Signal Input Terminals, Voltage[2]	–0.5V to (V+) + 0.5V
Current[2]	±10mA
Output Short Circuit[3]	Continuous
Operating Temperature	–40°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these, or any other conditions beyond those specified, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

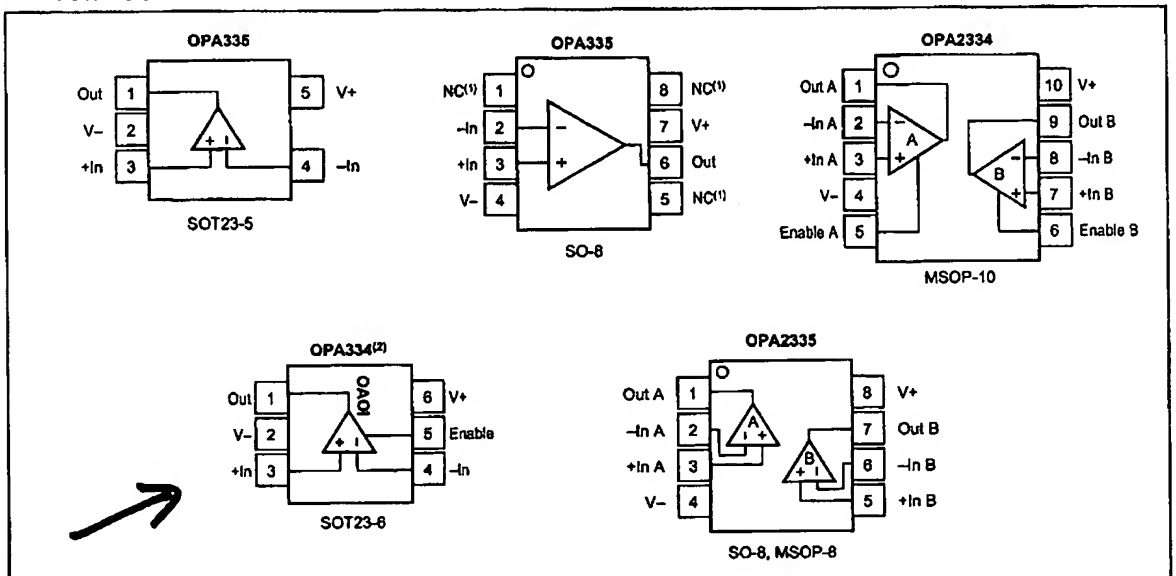
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
Shutdown Version						
OPA334AIDBV	SOT23-6	DBV	–40°C to +125°C	OAOI	OPA334AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA334AIDBVR	Tape and Reel, 3000
OPA2334AIDGS	MSOP-10	DGS	–40°C to +125°C	BHE	OPA2334AIDGST	Tape and Reel, 250
"	"	"	"	"	OPA2334AIDGSR	Tape and Reel, 2500
Non-Shutdown Version						
OPA335AIDBV	SOT23-5	DBV	–40°C to +125°C	OAPI	OPA335AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA335AIDBVR	Tape and Reel, 3000
OPA335AID	SO-8	D	–40°C to +125°C	OPA335	OPA335AID	Rails, 100
"	"	"	"	"	OPA335AIDR	Tape and Reel, 2500
OPA2335AID	SO-8	D	–40°C to +125°C	OPA2335	OPA2335AID	Rails, 100
"	"	"	"	"	OPA2335AIDR	Tape and Reel, 2500
OPA2335AIDGK	MSOP-8	DGK	–40°C to +125°C	BHF	OPA2335AIDGKT	Tape and Reel, 250
"	"	"	"	"	OPA2335AIDGKR	Tape and Reel, 2500

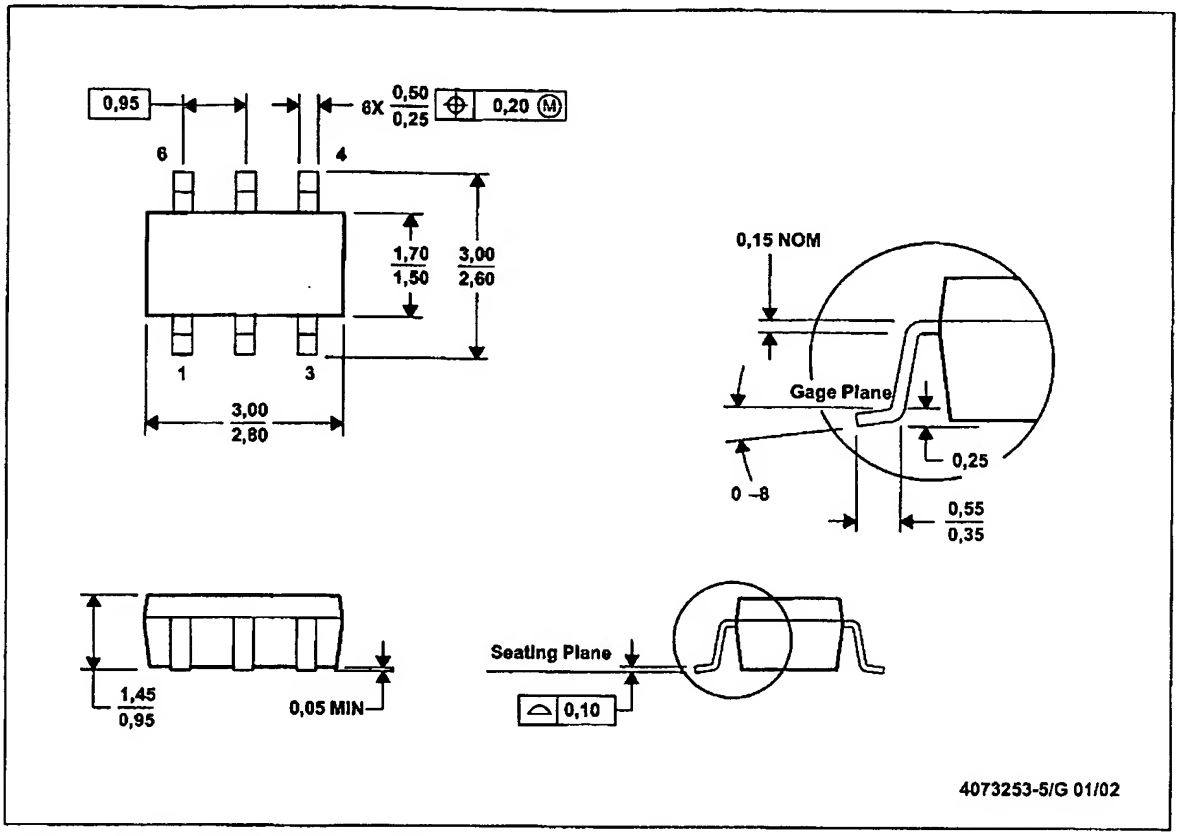
NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATIONS



NOTES: (1) NC indicates no internal connection. (2) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram.

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.